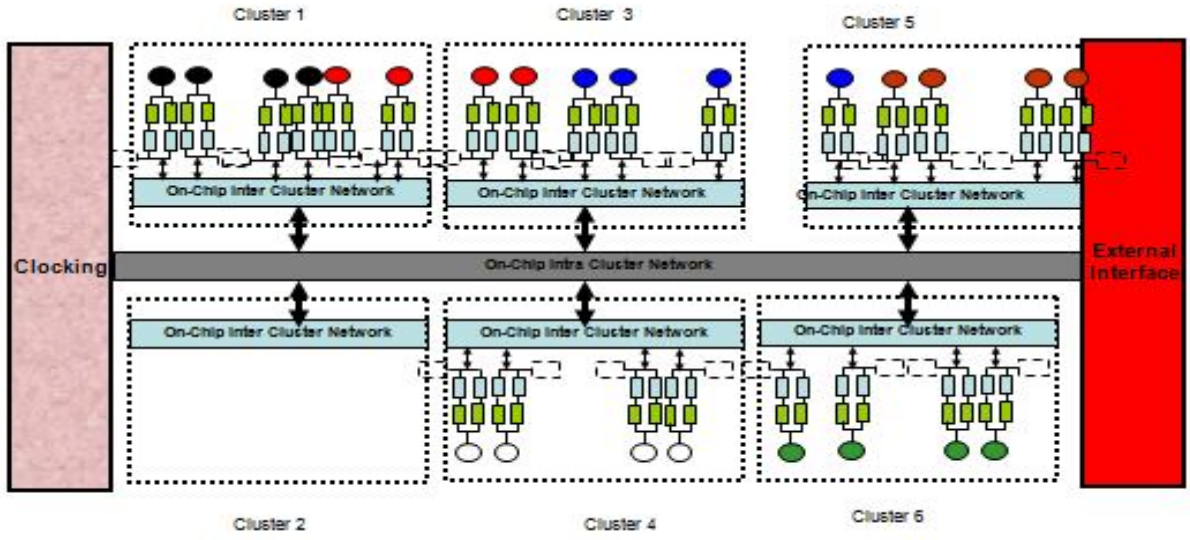

Fig. 1: Architecture of HMPM showing implementation of Processing-Stealing Technique after subjecting to workloads of 6:5:5:0:4:4 reconfiguration ratios

Legends

Cluster 1 Processing element

Cluster 2 Processing element

Cluster 3 Processing element

Cluster 4 Processing element

Level 1 Cache

Level 2 Cache

Cluster 5 Processing element

Cluster 6 Processing element

On Chip Inter Cluster Channel

On Chip Intra Cluster Channel